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SystemVerilog – Unified Hardware Design, Specification, and Verification Language

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SystemVerilog – Unified Hardware Design, Specification, and Verification Language

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This second edition cancels and replaces the first edition published in 2007. This edition constitutes a technical revision.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1800 (2009)	93/303/FDIS	93/305/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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IEEE Standard for SystemVerilog — Unified Hardware Design, Specification, and Verification Language

Sponsor
Design Automation Standards Committee
of the
IEEE Computer Society

and the
IEEE Standards Association Corporate Advisory Group

Approved 11 November 2009
IEEE-SA Standards Board

Abstract: This standard represents a merger of two previous standards: IEEE Std 1364™-2005 Verilog hardware description language (HDL) and IEEE Std 1800-2005 SystemVerilog unified hardware design, specification, and verification language. The 2005 SystemVerilog standard defines extensions to the 2005 Verilog standard. These two standards were designed to be used as one language. Merging the base Verilog language and the SystemVerilog extensions into a single standard provides users with all information regarding syntax and semantics in a single document.

Keywords: assertions, design automation, design verification, hardware description language, HDL, HDVL, PLI, programming language interface, SystemVerilog, Verilog, VPI

IEEE introduction

The purpose of this standard is to provide the electronic design automation (EDA), semiconductor, and system design communities with a well-defined and official IEEE unified hardware design, specification, and verification standard language. The language is designed to coexist and enhance the hardware description and verification languages (HDVLs) presently used by designers while providing the capabilities lacking in those languages.

SystemVerilog is a unified hardware design, specification, and verification language based on the Accellera SystemVerilog 3.1a extensions to the Verilog HDL [B3][a], published in 2004. Accellera is a consortium of EDA, semiconductor, and system companies. IEEE Std 1800 enables a productivity boost in design and validation and covers design, simulation, validation, and formal assertion-based verification flows.

SystemVerilog enables the use of a unified language for abstract and detailed specification of the design, specification of assertions, coverage, and testbench verification based on manual or automatic methodologies. SystemVerilog offers application programming interfaces (APIs) for coverage and assertions, a vendor-independent API to access proprietary waveform file formats, and a direct programming interface (DPI) to access proprietary functionality. SystemVerilog offers methods that allow designers to continue to use present design languages when necessary to leverage existing designs and intellectual property. This standardization project will provide the VLSI design engineers with a well-defined IEEE standard, which meets their requirements in design and validation, and which enables a step function increase in their productivity. This standardization project will also provide the EDA industry with a standard to which they can adhere and which they can support in order to deliver their solutions in this area.

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[a]The numbers in brackets correspond to the numbers in the bibliography in Annex R.

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