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Behavioural languages –
Part 1-1: VHDL Language Reference Manual

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1076 (2019)	91/1871/FDIS	91/1885/RVD

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IEEE Std 1076™-2019
(Revision of
IEEE Std 1076-2008)

IEEE Standard for VHDL Language Reference Manual

Developed by the

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 5 September 2019

IEEE SA Standards Board

Abstract: VHSIC Hardware Description Language (VHDL) is defined. VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. Its primary audiences are the implementors of tools supporting the language and the advanced users of the language.

Keywords: computer languages, electronic systems, hardware, hardware design, IEEE 1076™, VHDL

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This introduction is not part of IEEE Std 1076-2019, IEEE Standard for VHDL Language Reference Manual.

The VHSIC Hardware Description Language (VHDL) is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware.

This document, IEEE Std 1076-2019, is a revision of IEEE Std 1076-2008. The IEEE VHDL Analysis and Standardization Group (VASG), otherwise known as the 1076 Working Group, gathered the requirements, developed language extensions, and completed a draft of this revised Language Reference Manual. That draft was returned to IEEE for final revision and approval, resulting in this document. This revision incorporates numerous enhancements, both major and minor, to previously existing language features and several new language features. The changes are summarized in Annex E. In addition, several VHDL library packages that were previously defined in separate standards are now defined in this standard, ensuring that they are treated as integral parts of the language. Finally, this revision incorporates the IEEE Property Specification Language (PSL) as part of VHDL. The combination of these changes significantly improves VHDL as a language for specification, design, and verification of complex electronic systems.

The maintenance of the VHDL language standard is an ongoing process. The chair of the VHDL Analysis and Standardization Group extends his gratitude to all who have participated in this revision and encourages the participation of all interested parties in future language revisions.[1]

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