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**SystemVerilog –
Part 2: Universal Verification Methodology Language Reference Manual**

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Contents

1.	Overview.....	13
1.1	Scope.....	13
1.2	Purpose.....	13
1.3	Conventions used.....	13
2.	Normative references.....	16
3.	Definitions, acronyms, and abbreviations.....	16
3.1	Definitions.....	16
3.2	Acronyms and abbreviations.....	17
4.	UVM class reference.....	18
5.	Base classes.....	20
5.1	Overview.....	20
5.2	uvm_void.....	20
5.3	uvm_object.....	20
5.4	uvm_transaction.....	31
5.5	uvm_port_base #(IF).....	36
5.6	uvm_time.....	40
6.	Reporting classes.....	43
6.1	Overview.....	43
6.2	uvm_report_message.....	43
6.3	uvm_report_object.....	46
6.4	uvm_report_handler.....	52
6.5	Report server.....	55
6.6	uvm_report_catcher.....	59
7.	Recording classes.....	65
7.1	uvm_tr_database.....	65
7.2	uvm_tr_stream.....	67
7.3	UVM links.....	71
8.	Factory classes.....	76
8.1	Overview.....	76
8.2	Factory component and object wrappers.....	76
8.3	UVM factory.....	82

9.	Phasing.....	89
9.1	Overview.....	89
9.2	Implementation.....	89
9.3	Phasing definition classes.....	89
9.4	uvm_domain.....	98
9.5	uvm_bottomup_phase.....	99
9.6	uvm_task_phase.....	100
9.7	uvm_topdown_phase.....	101
9.8	Predefined phases.....	102
10.	Synchronization classes.....	107
10.1	Event classes.....	107
10.2	uvm_event_callback.....	110
10.3	uvm_barrier.....	111
10.4	Pool classes.....	113
10.5	Objection mechanism.....	114
10.6	uvm_heartbeat.....	119
10.7	Callbacks classes.....	121
11.	Container classes.....	126
11.1	Overview.....	126
11.2	uvm_pool #(KEY,T).....	126
11.3	uvm_queue #(T).....	128
12.	UVM TLM interfaces.....	131
12.1	Overview.....	131
12.2	UVM TLM 1.....	131
12.3	UVM TLM 2.....	148
13.	Predefined component classes.....	168
13.1	uvm_component.....	168
13.2	uvm_test.....	181
13.3	uvm_env.....	182
13.4	uvm_agent.....	182
13.5	uvm_monitor.....	183
13.6	uvm_scoreboard.....	183
13.7	uvm_driver #(REQ,RSP).....	184
13.8	uvm_push_driver #(REQ,RSP).....	184
13.9	uvm_subscriber.....	185

14.	Sequences classes	187
14.1	uvm_sequence_item.....	187
14.2	uvm_sequence_base.....	191
14.3	uvm_sequence #(REQ,RSP).....	200
14.4	uvm_sequence_library	201
15.	Sequencer classes.....	206
15.1	Overview.....	206
15.2	Sequencer interface.....	206
15.3	uvm_sequencer_base	211
15.4	Common sequencer API	217
15.5	uvm_sequencer #(REQ,RSP).....	218
15.6	uvm_push_sequencer #(REQ,RSP).....	219
16.	Policy classes	220
16.1	uvm_policy	220
16.2	uvm_printer.....	222
16.3	uvm_comparer	237
16.4	uvm_recorder.....	243
16.5	uvm_packer.....	251
16.6	uvm_copier	257
17.	Register layer	260
17.1	Overview.....	260
17.2	Global declarations	260
18.	Register model	264
18.1	uvm_reg_block.....	264
18.2	uvm_reg_map.....	276
18.3	uvm_reg_file.....	284
18.4	uvm_reg	286
18.5	uvm_reg_field.....	303
18.6	uvm_mem	314
18.7	uvm_reg_indirect_data	328
18.8	uvm_reg_fifo	329
18.9	uvm_vreg.....	332
18.10	uvm_vreg_field.....	342
18.11	uvm_reg_cbs.....	347
18.12	uvm_mem_mam	352

19.	Register layer interaction with RTL design.....	361
19.1	Generic register operation descriptors.....	361
19.2	Classes for adapting between register and bus operations.....	365
19.3	uvm_reg_predictor.....	367
19.4	Register sequence classes.....	369
19.5	uvm_reg_backdoor.....	376
19.6	UVM HDL back-door access support routines.....	379
	Annex A (informative) Bibliography.....	381
	Annex B (normative) Macros and defines.....	382
	Annex C (normative) Configuration and resource classes.....	407
	Annex D (normative) Convenience classes, interface, and methods.....	422
	Annex E (normative) Test sequences.....	431
	Annex F (normative) Package scope functionality.....	443
	Annex G (normative) Command line arguments.....	466
	Annex H (informative) Participants.....	471

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Keywords: agent, blocking, callback, class, component, consumer, driver, event, export, factory, function, generator, IEEE 1800.2™, member, method, monitor, non-blocking, phase, port, register, resource, sequence, sequencer, transaction level modeling, verification methodology

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Introduction

This introduction is not part of IEEE Std 1800.2-2017, IEEE Standard for Universal Verification Methodology Language Reference Manual.

Verification has evolved into a complex project that often spans internal and external teams, but the discontinuity associated with multiple, incompatible methodologies among those teams can limit productivity. The Universal Verification Methodology (UVM) Language Reference Manual (LRM) addresses verification complexity and interoperability within companies and throughout the electronics industry for both novice and advanced teams while also providing consistency. While UVM is revolutionary, being the first verification methodology to be standardized, it is also evolutionary, as it is built on the Open Verification Methodology (OVM), which combined the Advanced Verification Methodology (AVM) with the Universal Reuse Methodology (URM) and concepts from the *e* Reuse Methodology (eRM). Furthermore, UVM also infuses concepts and code from the Verification Methodology Manual (VMM), plus the collective experience and knowledge of the over 300 members of the Accellera UVM Working Group to help standardize verification methodology. Finally, the transaction level modeling (TLM) facilities in UVM are based on what was developed by Open SystemC Initiative (OSCI) for SystemC, though they are not an exact replication or re-implementation of the SystemC TLM library.

Withdrawal