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Environmental and endurance testing – Test methods for surface-mount boards of area array type packages FBGA, BGA, FLGA, LGA, SON and QFN

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

ENVIRONMENTAL AND ENDURANCE TESTING – TEST METHODS FOR SURFACE-MOUNT BOARDS OF AREA ARRAY TYPE PACKAGES FBGA, BGA, FLGA, LGA, SON AND QFN[1]

FOREWORD

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International Standard IEC 62137 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/444/FDIS	91/451/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

1 FBGA fine-pitch ball grid array
BGA ball grid array
FLGA fine-pitch land grid array
LGA land grid array
SON small outline non-leaded package
QFN quad flat-pack non-leaded package

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version may be issued at a later date.

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ENVIRONMENTAL AND ENDURANCE TESTING – TEST METHODS FOR SURFACE-MOUNT BOARDS OF AREA ARRAY TYPE PACKAGES FBGA, BGA, FLGA, LGA, SON AND QFN

1 Scope

This International Standard specifies the test method and guidelines for evaluating the quality and reliability of boards, solder lands, solder process and solder joints of reflow solder mounted area array type packages and peripheral terminal type packages.

This standard tests for durability against mechanical and thermal stress received during or after the mounting process of discrete semiconductor devices and of integrated circuits (hereinafter both referred to as semiconductor devices) used mainly for industrial and consumer use equipment.

The test method specified in this standard is an integrated one by including the evaluation method of mounting methods, mounting conditions, printed circuit boards, soldering materials, and so on. It does not specify the evaluation method of the individual semiconductor devices.

Mounting conditions, printed wiring boards, soldering materials, and so on significantly affect the result of the test specified in this standard. Therefore, the test specified in this standard shall not be regarded as the one to be used to guarantee the mounting reliability of the semiconductor devices.

The test method is not necessary if there is no stress (mechanical or others) from any of the tests covered in this standard.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-1:1988, *Environmental testing – Part 1: General and guidance*

IEC 60191-6-2:2001, *Mechanical standardization of semiconductor devices – Part 6-2: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for 1,50 mm, 1,27 mm and 1,00 mm pitch ball and column terminal packages*

IEC 60191-6-5:2001, *Mechanical standardization of semiconductor devices – Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)*

IEC 61190-1-1, *Attachment materials for electronic assemblies – Part 1-1: Requirements for soldering fluxes for high-quality interconnections in electronics assembly*

IEC 61190-1-2, *Attachment materials for electronic assemblies – Part 1-2: Requirements for solder pastes for high-quality interconnections in electronics assembly*

IEC 61190-1-3, *Attachment materials for electronic assemblies – Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solders for electronic soldering applications*

JEITA[2] ETR-7001:1998, *Terms and definitions for surface mount technology*

[2] Japan Electronics and Information Technology Industries Association.

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